GIET
In Pursuit of Innovation

GIETPOLYTECHNIC,JAGATPUR,CUTTACK

LESSONPLAN

Discipline: ETC.	Semester:- 3rd	Name of the Teaching Faculty:- Pradeepta prajnaranjan swain.
Subject:-DIGITAL ELECTRONICS. [TH-3]	No of Days/per Week Class Allotted: 03	Semester-3rd From:01.07.2026 To:05.11.2026 No of Weeks:-15
Week	**Class/Day**	**Theory Topics**
1st	1st	**Logic Gates** 1.1 Basic logic gates: OR, AND, and NOT (1) Truth tables (2) Logic symbols
	2nd	(3)Logic voltage levels (4) Logic circuit design examples
	3rd	(4) NOR and NAND gates used as inverters. (5) Fan-in and fan-out 1.6 Termination of unused inputs 1.7 AND and OR gates constructed From NAND and NOR gates
2nd	1st	(4) NOR and NAND gates used as inverters. (5) Fan-in and fan-out
	2nd	(6)Termination of unused inputs (7) AND and OR gates constructed From NAND and NOR gates
	3rd	6)Termination of unused inputs (7) AND and OR gates constructed From NAND and NOR gates
3rd	1st	6)Termination of unused inputs (7) AND and OR gates constructed From NAND and NOR gates
	2nd	6)Termination of unused inputs (7) AND and OR gates constructed From NAND and NOR gates
	3rd	Doubt clearing class.
4th	1st	**Boolean Algebra** (1)Boolean operations (OR, AND, NOT)((2) Representation of logic circuits by Boolean expressions.
	2nd	(3) Laws of Boolean algebra: (4) Double inversion: A"=A
	3rd	5) OR identities: A+0 = A, A+1=1, A+A=A, A+A'=1 (6) AND identities: A.0=0, A.1=A, A.A=A, A.A'=0 (7)4 Cumulative laws: A+B=B+A, A.B=B.A (8) Associative laws:(A+B)+C=A+(B+C), (A.B).C=A.(B.C) (9) Distributive laws: A+(B.C)=(A+B).(A+C), A.(B+C)=A.B+A.C (10) Demerger's theorems :(A+B+C+...)'=A'.B'.C'...,(A.B.C...)'=A'+B'+C'... 2.3.8 Applications to logic circuit simplifications and design.
5th	1st	11) Equivalent logic gates (12) NAND and NOR implementations of logic circuits.
	2nd	(11) Equivalent logic gates (12) NAND and NOR implementations of logic circuits.
	3rd	11) Equivalent logic gates (12) NAND and NOR implementations of logic circuits.
6th	1st	11) Equivalent logic gates (12) NAND and NOR implementations of logic circuits.
	2nd	11) Equivalent logic gates (12) NAND and NOR implementations of logic circuits.

	3rd	(14)1 Sum-of-products (SOP) 2.6.2 Product-of-sums (POS). (15)Karnaugh mapping
7th	1st	(15)Karnaugh mapping
	2nd	(15)Karnaugh mapping
	3rd	(15)Karnaugh mapping
8th	1st	**Combinational Logic Circuits.** (1)Half adder (2) Full adder
	2nd	(3) Half Subtractor (4) Full Subtractor
	3rd	(5) 4 bit adder. (6) Multiplexer (4:1) (7) De- multiplexer (1:4)
9th	1st	(8) Decoder (9)Encoder
	2nd	(10) Digital comparator (3 Bit) (11) Seven segment Decoder
	3rd	Doubt clearing class
10th	1st	**Latches & Flip-Flops** (1)Basic latches (2)NOR latch (3)NAND latch (4)Exampleuses of latches
	2nd	(5)Gated latches (6) Gated S-R latch (7) Gated D-latch
	3rd	(8)Flip-flops: (9) Master-slave and edge-triggered principles (10) S-R flip-flop (11) D-type flip-flop
11th	1st	12) J-K flip-flop (13) T-type flip-flop (14) Flip-flop timing diagrams
	2nd	**Counters** (1)Circuit diagram and working principle of Binary counters (2)up-down counter (circuits, truth tables, and timing diagrams) (3)Asynchronous counters and ripple counter (4)Synchronous counters
	3rd	(4)Synchronous counters (5)Decade counter (6)Module–n counter and its combinations
12th	1st	(7)Divide-by-n counters obtained from truncated binary sequences (8)Synchronous counter design using D-type flip-flops (9)Synchronous counter design using J-K flip-flops
	2nd	**Shift Registers** (1) Circuit diagram, truth tables, and timing diagrams of Shift Registers (2)Serial input shift register (3)Serial/parallel load shift register (4)Shift register counters
	3rd	(5)Ring counter (6)Self-starting ring counter (7)Johnson counter
13th	1st	**Semiconductor Memories** (1) Define the terms ROM, RAM, PROM, EPROM. (2) Draw typical memory cell (3) Design a small diode matrix ROM to serve as a code converter. (4) Design and draw the logic diagram of a specified size memory system
	2nd	(5) Operating principle of dynamic memory (6) Advantages and disadvantages of dynamic memory vs. static memory (7) Difference between dynamic memory vs. static memory
	3rd	**Sequential Circuit Design** (1) Combinational vs. Sequential circuits (2)Adder, Subtractor, decoder, multiplexer, de-multiplexer, and comparator
	1st	(3)Finite state machines- Concept only

14th	2nd	Class test
	3rd	Doubt clearing class.
15th	1st	Doubt clearing class.
	2nd	Doubt clearing class.
	3rd	Doubt clearing class.

Pradeepta Prajnaranjan Swain.
Sign. of faculty

24.6.26
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